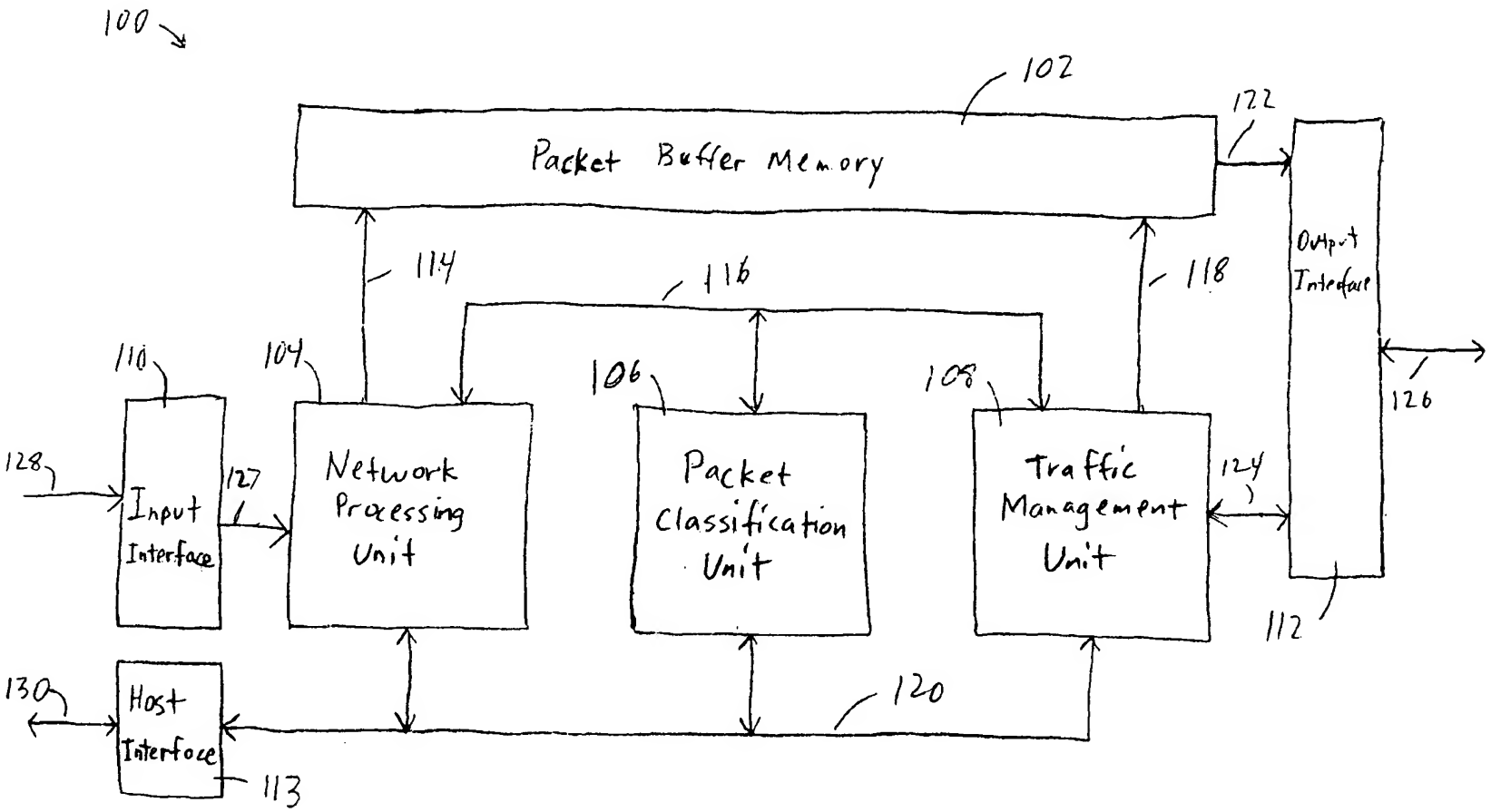
100
102
Packet Buffer Memory
122
Output Interface
126
114
116
118
110
104
106
108
Input Interface
127
Network Processing Unit
Packet Classification Unit
Traffic Management Unit
124
128
112
130
Host Interface
113
120

FIG. 1

200

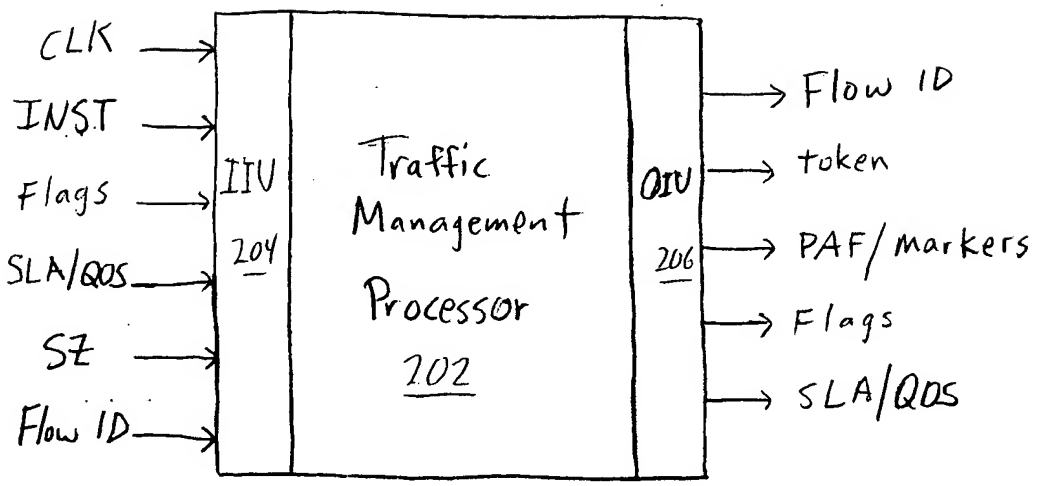

FIG. 2

300

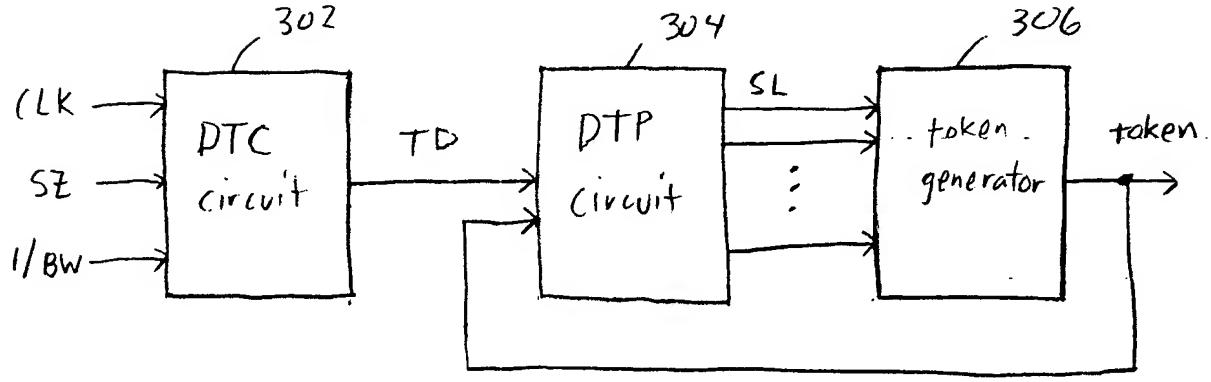

FIG. 3

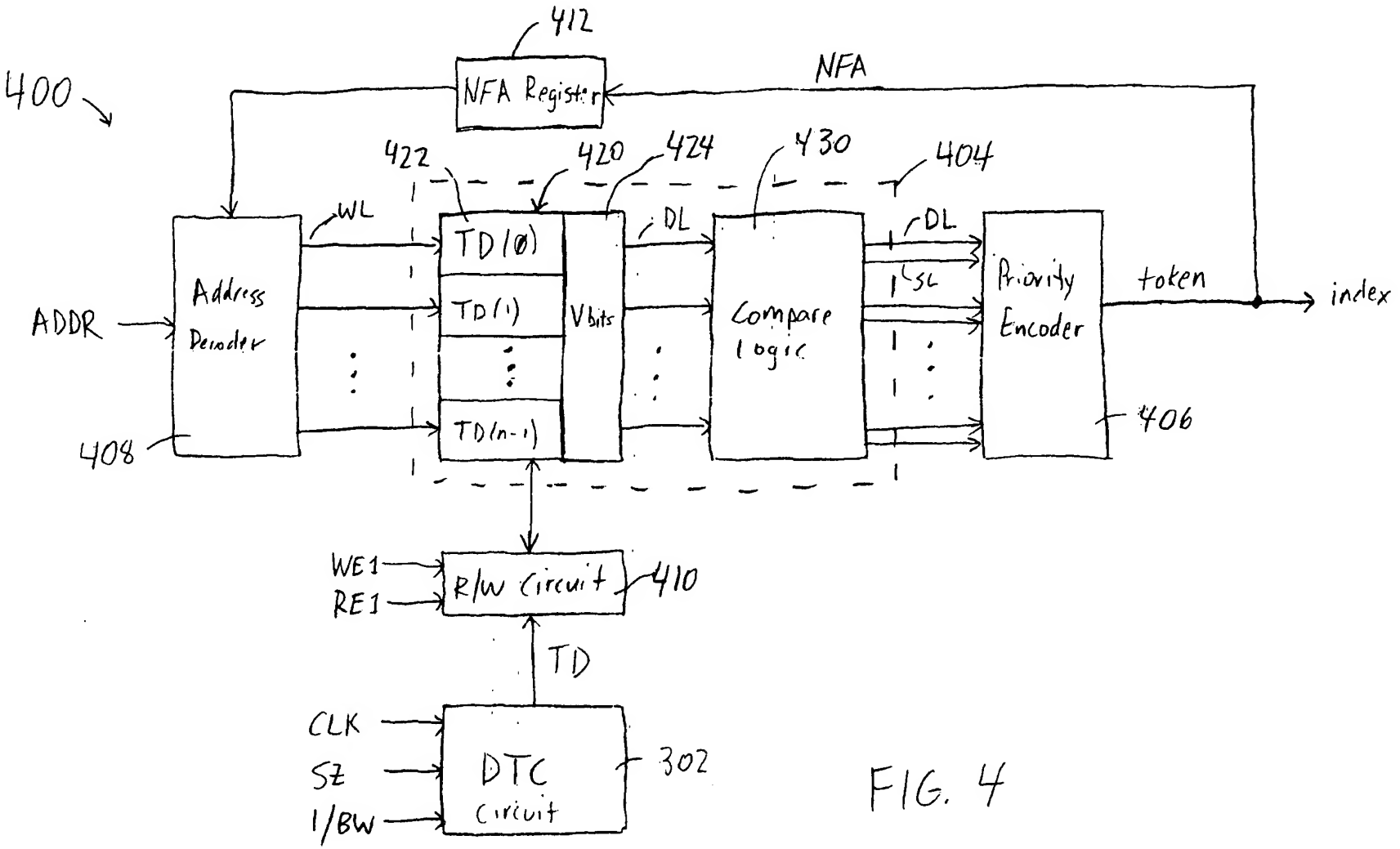
400
412
NFA Register
NFA
422
420
424
430
404
WL
DL
DL
TD(0)
TD(1)
TD(n-1)
Vbits
Address Decoder
ADDR
408
Compare Logic
SL
Priority Encoder
token
index
406
WE1
RE1
R/W Circuit
410
TD
CLK
SE
I/BW
DTC Circuit
302

FIG. 4

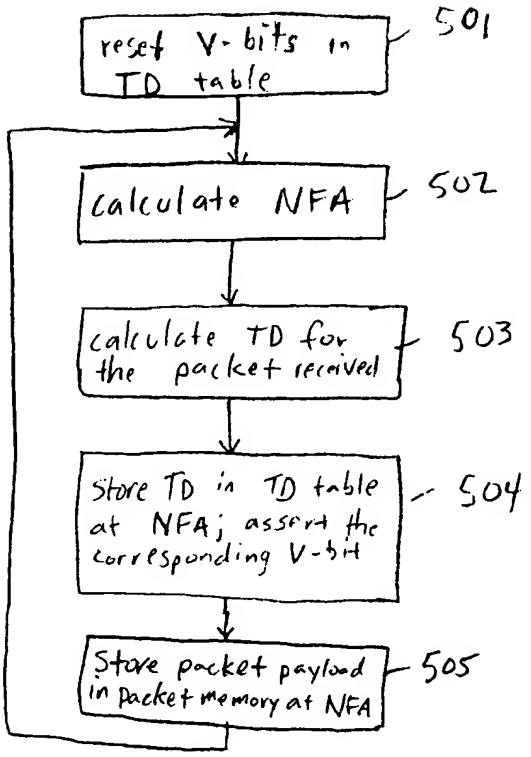

FIG. 5A

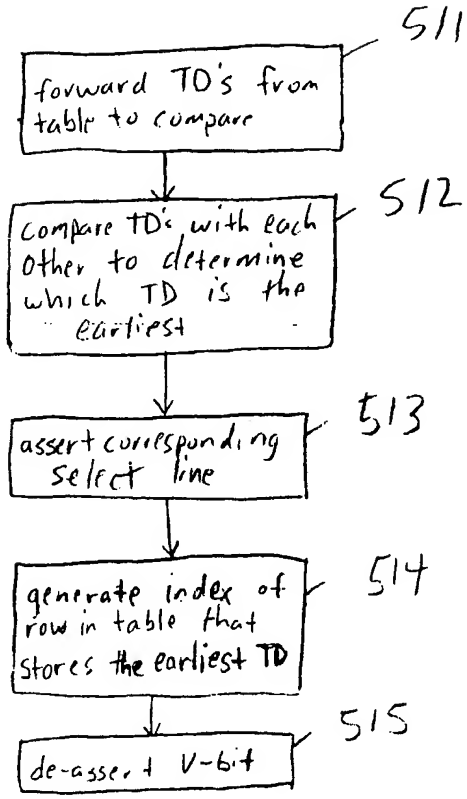

FIG. 5B

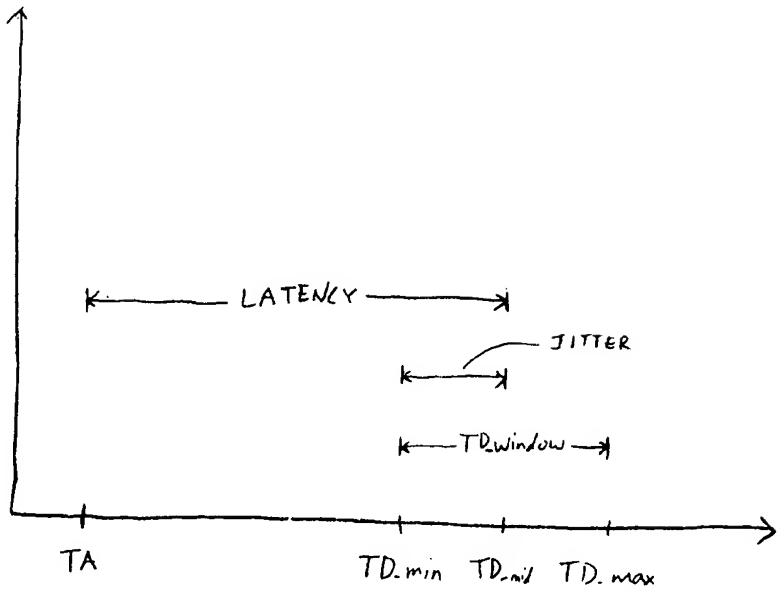

FIG. 6

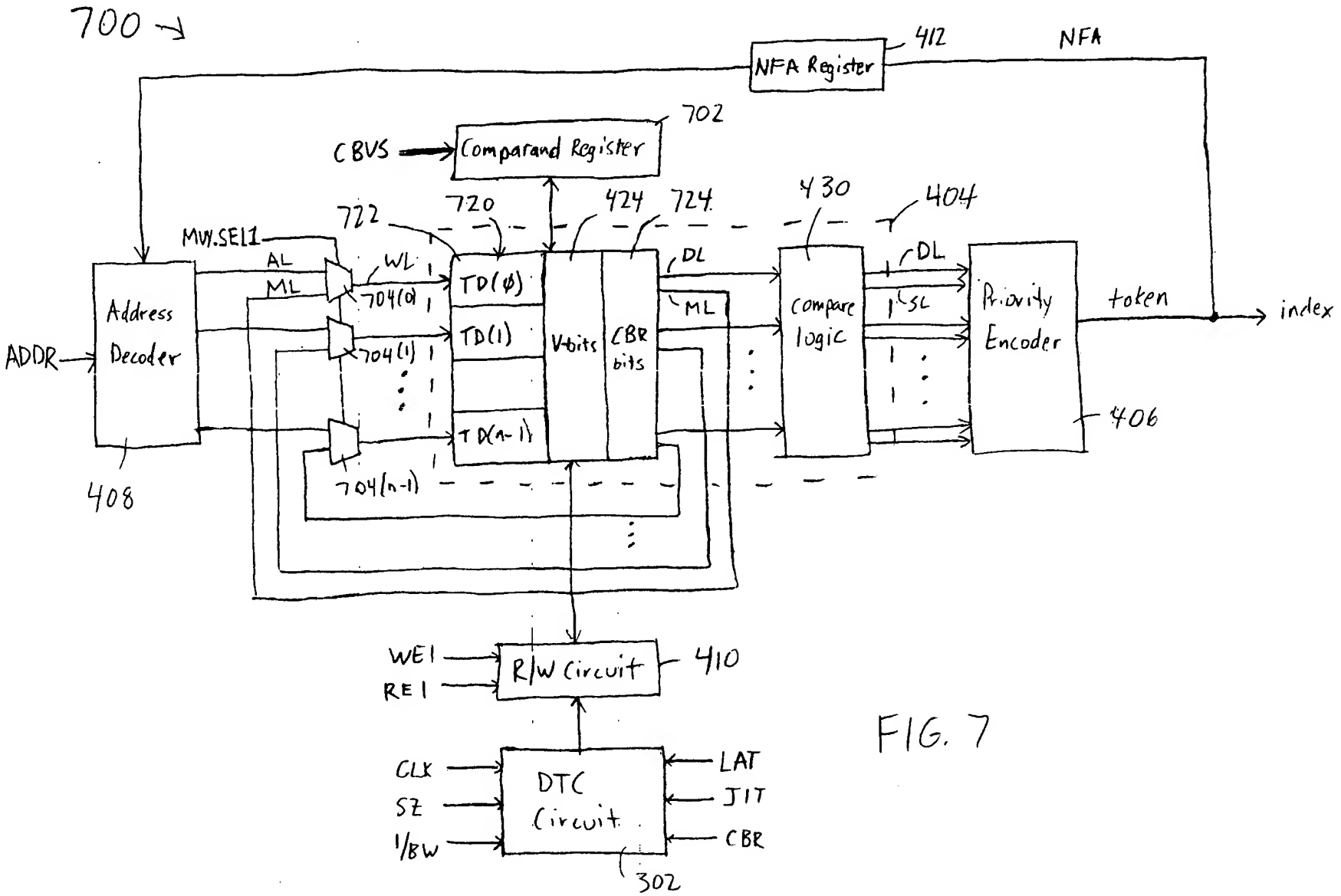
700
NFA Register
412
NFA
702
CBUS
Comparand Register
722
720
424
724
430
404
MW.SEL1
AL
ML
WL
TD(0)
TD(1)
TD(n-1)
V-bits
CBR bits
DL
ML
Compare logic
SL
Priority Encoder
token
index
ADDR
Address Decoder
704(0)
704(1)
704(n-1)
408
406
WE1
RE1
R/W Circuit
410
CLK
SZ
I/BW
DTC Circuit
LAT
JIT
CBR
302

FIG. 7

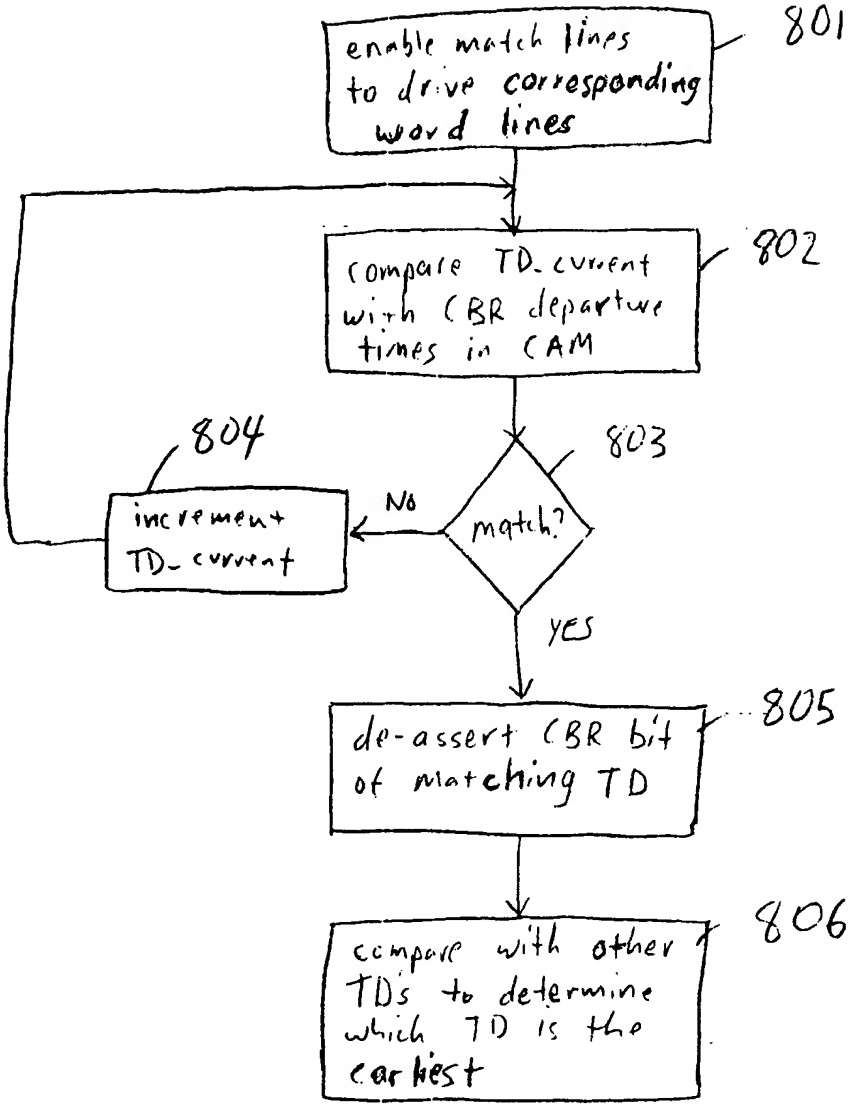
enable match lines to drive corresponding word lines
801
compare TD_current with CBR departure times in CAM
802
match?
803
No
increment TD_current
804
yes
de-assert CBR bit of matching TD
805
compare with other TDs to determine which TD is the earliest
806

FIG. 8

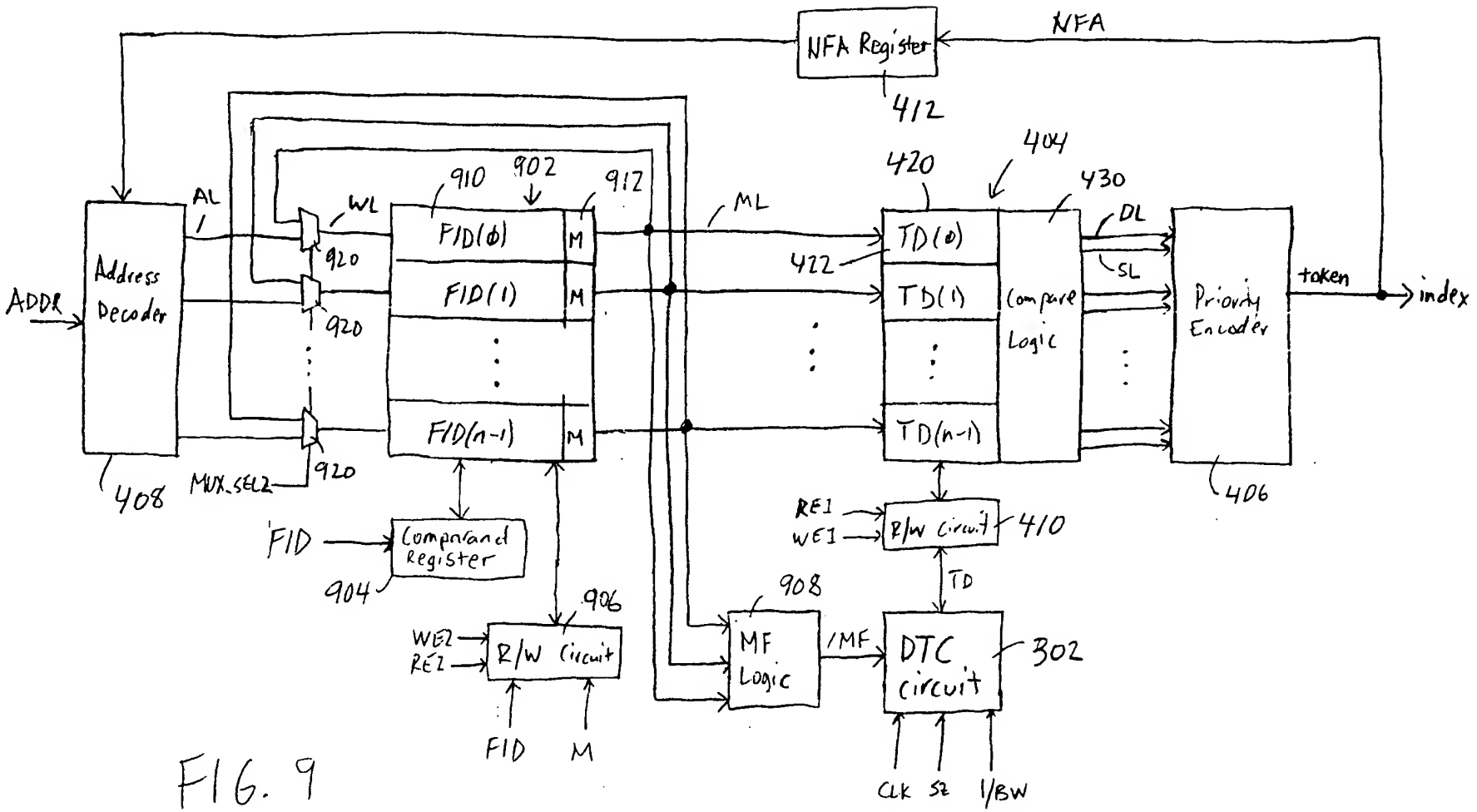
900
NFA Register
NFA
412
404
420
430
910
902
912
AL
WL
ML
DL
SL
ADDR
Address Decoder
920
FID(0)
FID(1)
FID(n-1)
M
TD(0)
TD(1)
TD(n-1)
422
Compare Logic
Priority Encoder
token
index
408
MUX_SEL2
406
FID
Comparand Register
904
RE1
WE1
R/W circuit
410
TD
908
906
WE2
RE2
MF Logic
/MF
DTC circuit
302
FID
M
CLK
S2
1/BW

FIG. 9

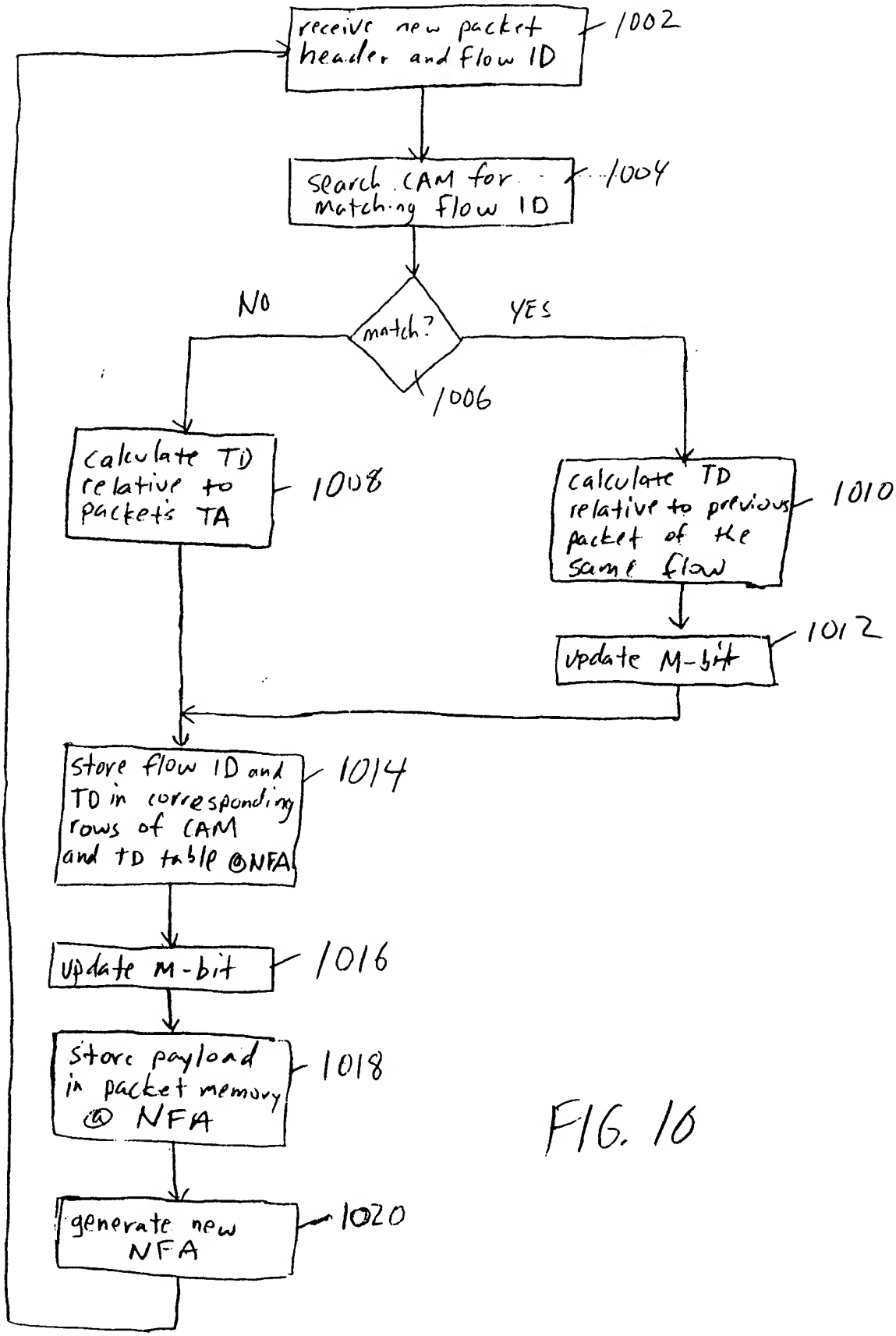
receive new packet header and flow ID
1002
search CAM for matching flow ID
1004
match?
1006
NO
YES
calculate TD relative to packet's TA
1008
calculate TD relative to previous packet of the same flow
1010
update M-bit
1012
store flow ID and TD in corresponding rows of CAM and TD table @ NFA
1014
update M-bit
1016
store payload in packet memory @ NFA
1018
generate new NFA
1020

FIG. 10

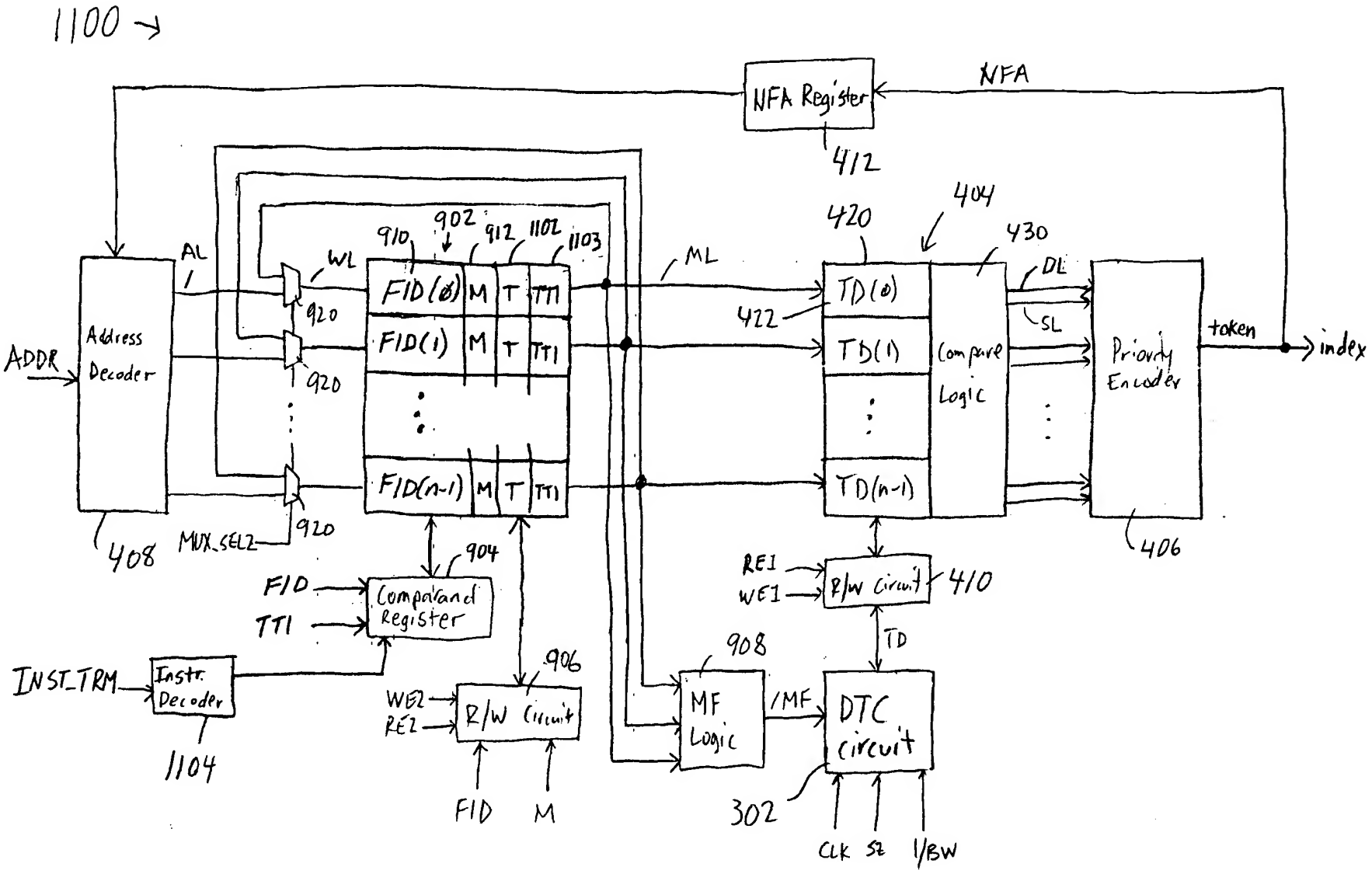
1100
NFA Register
NFA
412
404
420
430
910
902
912
1102
1103
WL
AL
ML
DL
SL
ADDR
Address Decoder
920
FID(0)
M
T
TTI
FID(1)
FID(n-1)
TD(0)
TD(1)
TD(n-1)
422
Compare Logic
Priority Encoder
token
index
408
MUX_SEL2
406
904
FID
TTI
Comparand Register
RE1
WE1
R/W Circuit
410
TD
INST_TRM
Instr. Decoder
1104
906
908
WE2
RE2
R/W Circuit
MF Logic
/MF
DTC circuit
302
FID
M
CLK
S2
1/BW

FIG. 11

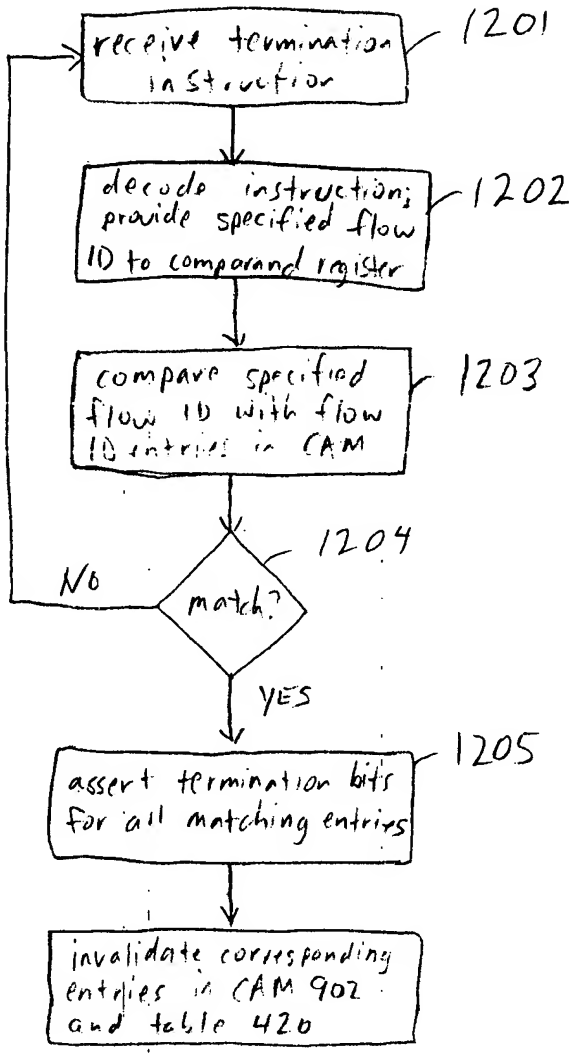

FIG. 12A

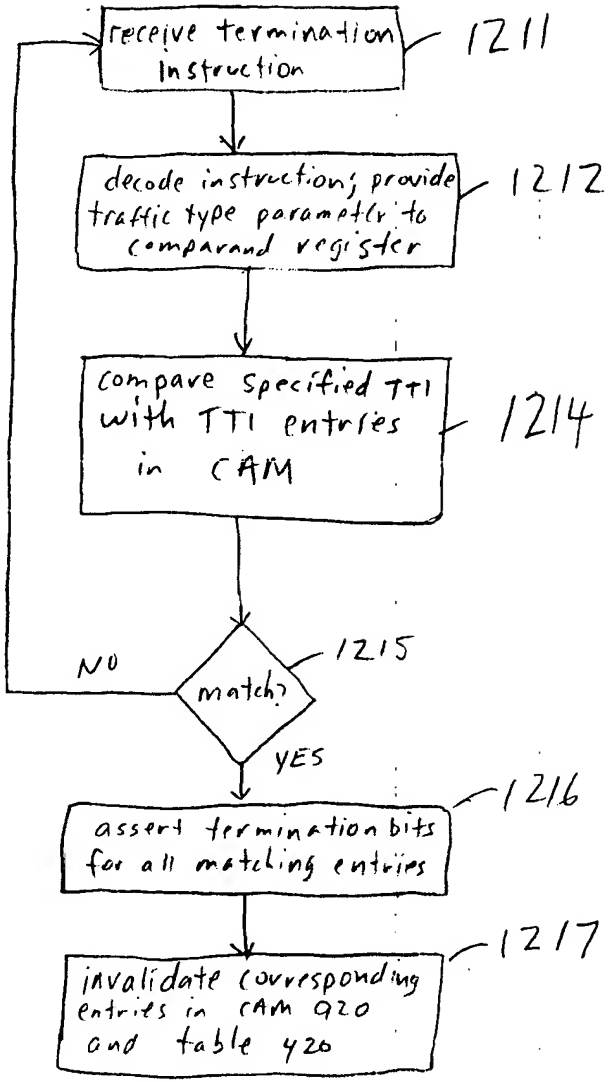

FIG. 12B

1300 →

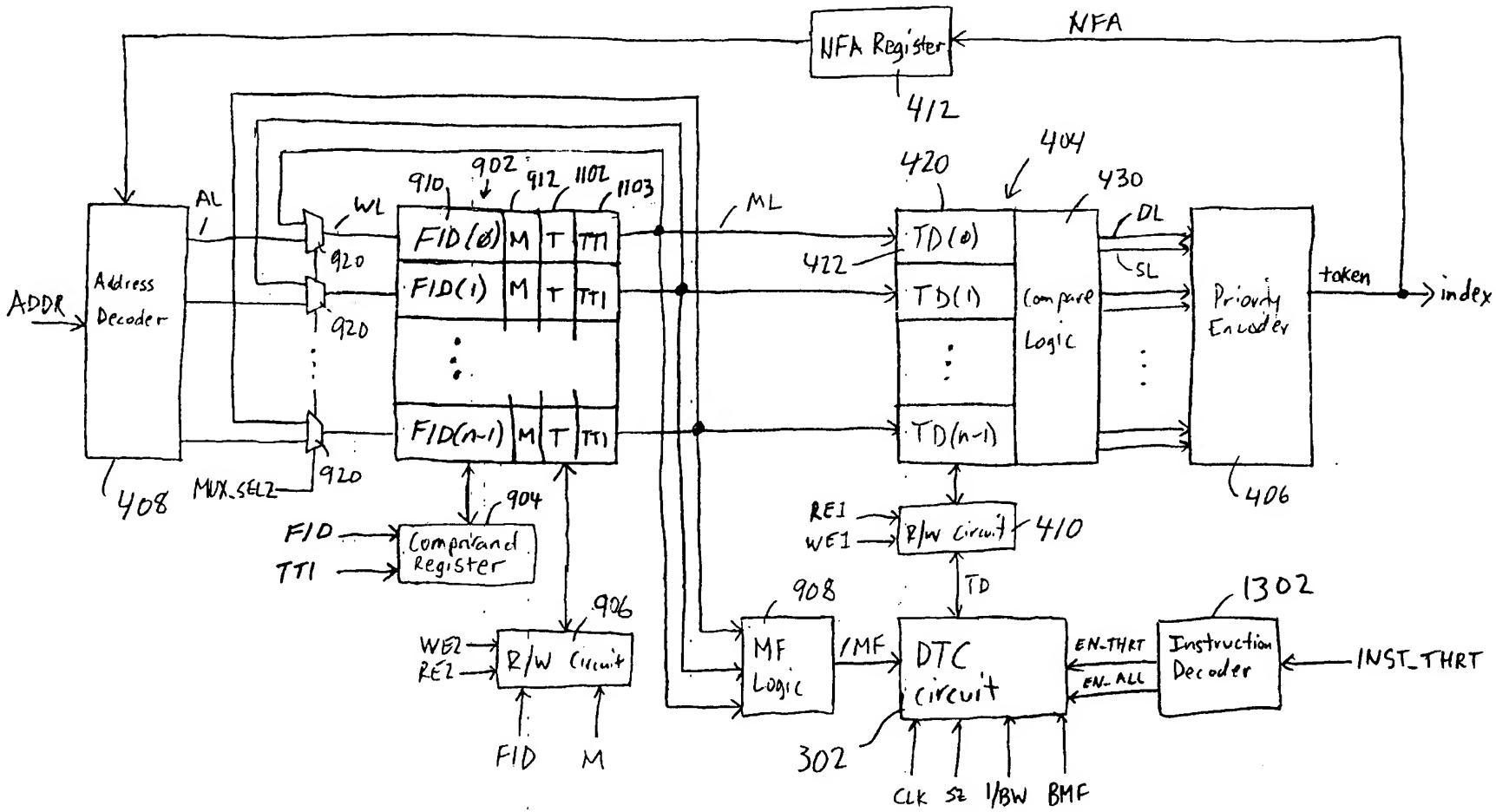
NFA Register
NFA
412
404
420
430
902
910
912
1102
1103
WL
AL
ML
DL
SL
ADDR
Address Decoder
920
FID(0)
M
T
TTI
FID(1)
FID(n-1)
TD(0)
TD(1)
TD(n-1)
Compare Logic
Priority Encoder
taken
index
422
408
MUX_SEL2
904
FID
TTI
Comparand Register
RE1
WE1
R/W circuit
410
406
TD
908
906
1302
WE2
RE2
MF Logic
/MF
DTC circuit
EN_THRT
EN_ALL
Instruction Decoder
INST_THRT
302
CLK
S2
I/BW
BMF

FIG. 13

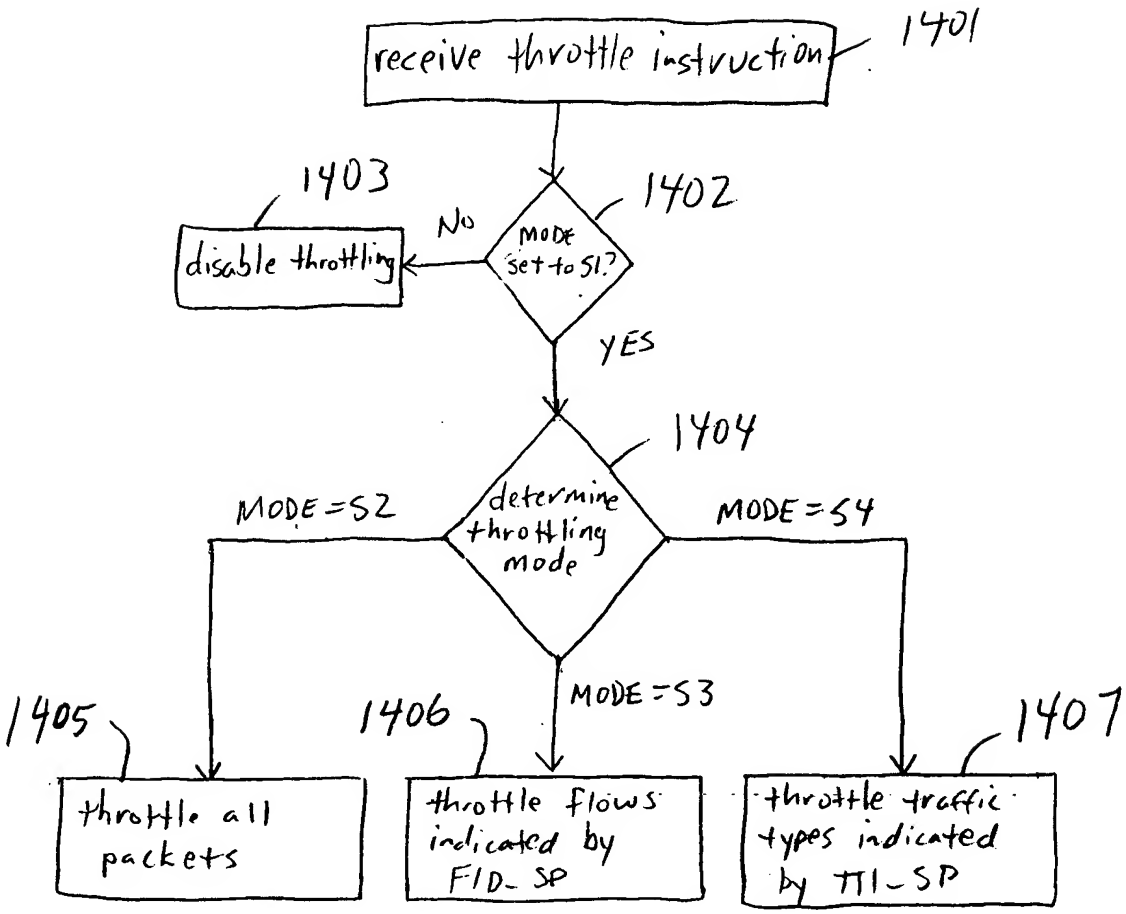
receive throttle instruction
1401
1403
1402
No
disable throttling
MODE set to S1?
YES
1404
MODE=S2
determine throttling mode
MODE=S4
MODE=S3
1405
1406
1407
throttle all packets
throttle flows indicated by FID_SP
throttle traffic types indicated by TTI_SP

FIG. 14

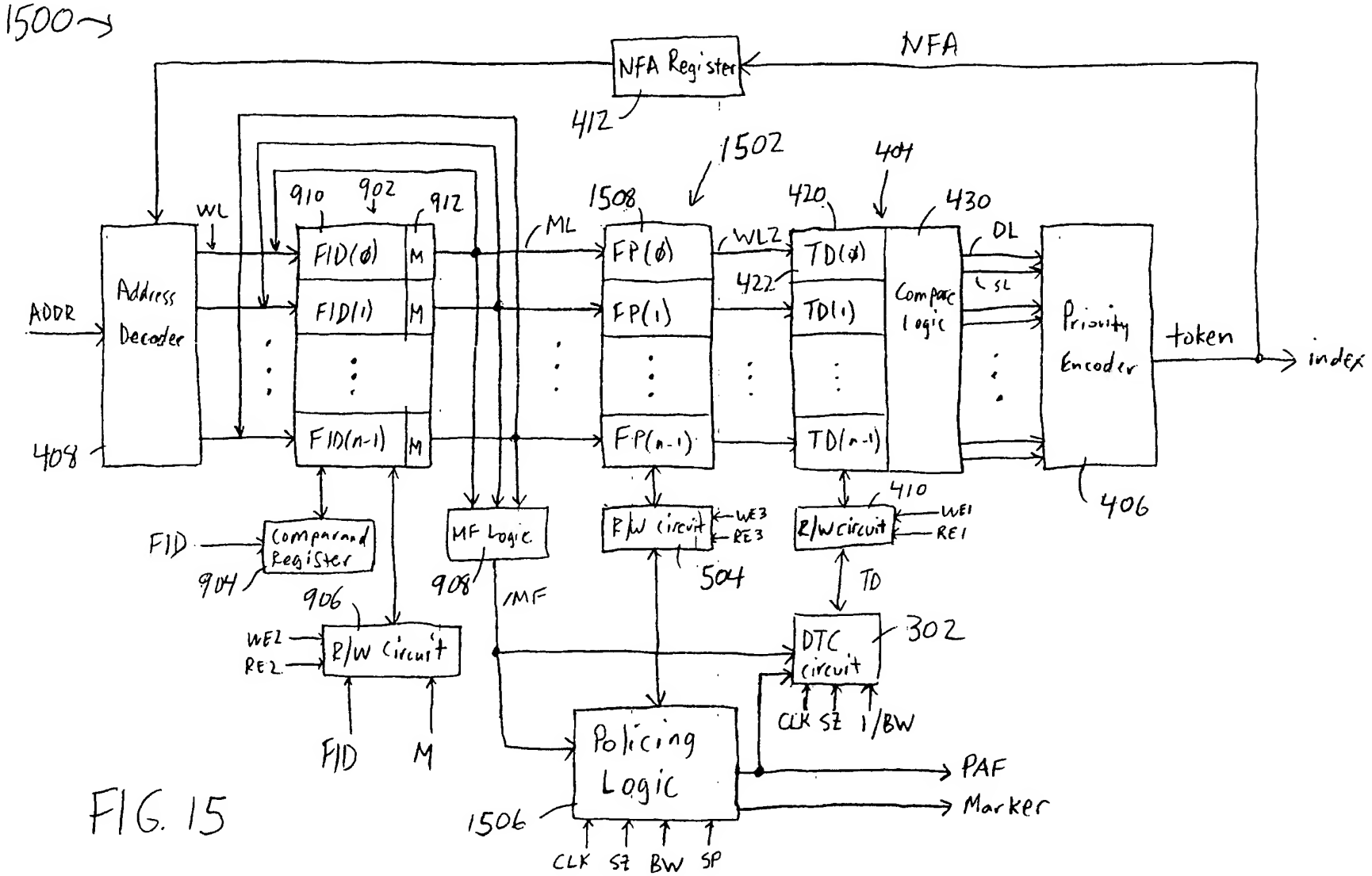
1500
NFA Register
NFA
412
1502
404
910
902
912
1508
420
430
WL
ML
WL2
DL
422
ADDR
Address Decoder
FID(0)
FID(1)
FID(n-1)
M
FP(0)
FP(1)
FP(n-1)
TD(0)
TD(1)
TD(n-1)
Compare Logic
Priority Encoder
token
index
408
406
410
FID
Comparand Register
904
MF Logic
908
R/W circuit
WE3
RE3
WE1
RE1
504
TD
906
WE2
RE2
MF
DTC circuit
302
CLK
SZ
1/BW
Policing Logic
PAF
Marker
1506
CLK
SZ
BW
SP

FIG. 15

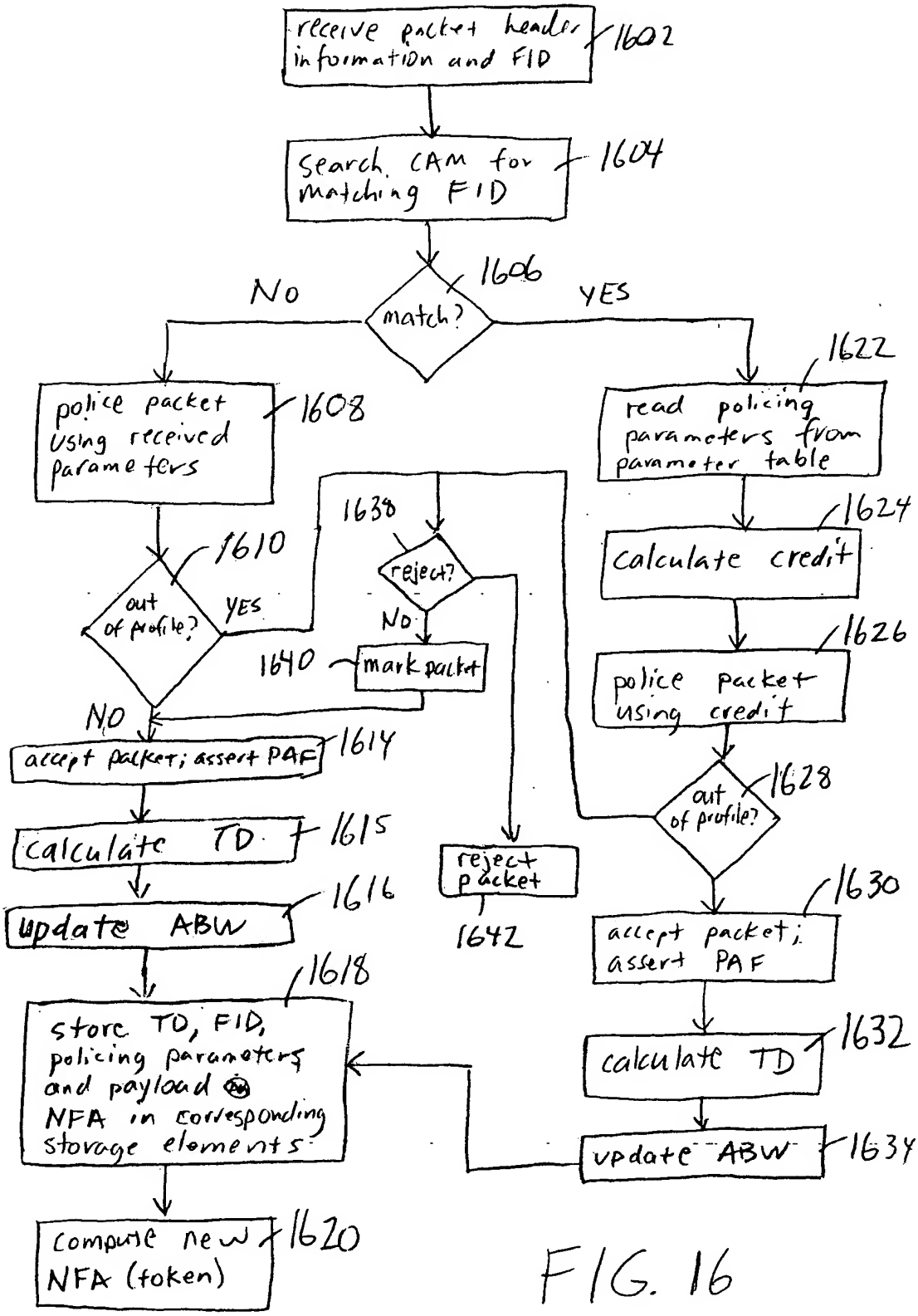
receive packet header information and FID
1602
search CAM for matching FID
1604
match?
1606
NO
YES
police packet using received parameters
1608
out of profile?
1610
YES
NO
1630
reject?
NO
1640
mark packet
accept packet; assert PAF
1614
calculate TD
1615
update ABW
1616
store TD, FID, policing parameters and payload & NFA in corresponding storage elements
1618
compute new NFA (token)
1620
reject packet
1642
read policing parameters from parameter table
1622
calculate credit
1624
police packet using credit
1626
out of profile?
1628
accept packet; assert PAF
1630
calculate TD
1632
update ABW
1634

FIG. 16

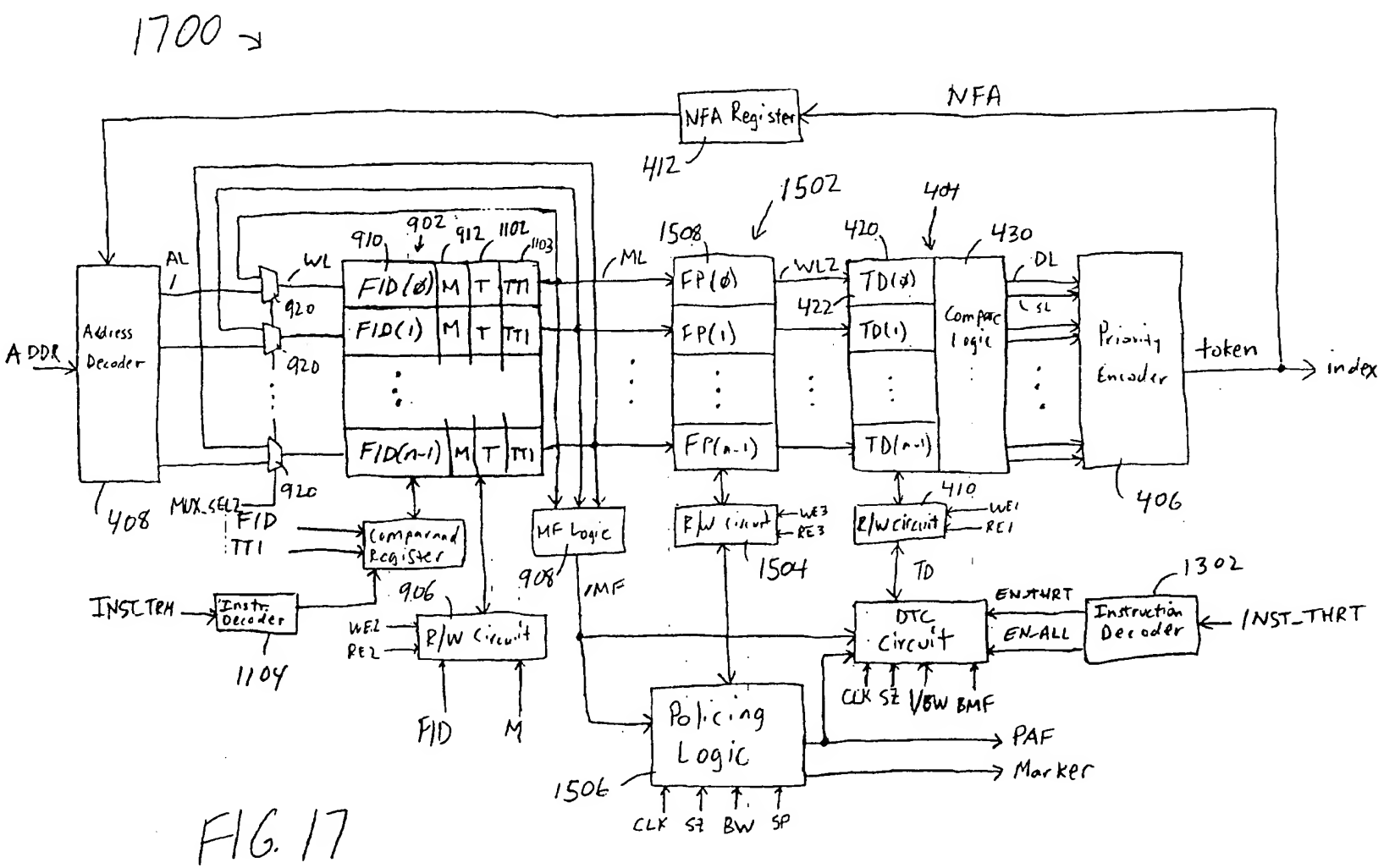
1700
NFA Register
NFA
412
1502
401
1508
420
430
910
902
912
1102
1103
AL
WL
ML
WL2
DL
CSL
ADDR
Address Decoder
FID(0)
FID(1)
FID(n-1)
M
T
TT1
920
422
FP(0)
FP(1)
FP(n-1)
TD(0)
TD(1)
TD(n-1)
Compare Logic
Priority Encoder
token
index
408
406
410
MUX_SEL2
FID
TT1
Compared Register
MF Logic
908
1MF
R/W circuit
WE3
RE3
WE1
RE1
1504
TD
1302
INST_THRT
Instr. Decoder
1104
906
WE2
RE2
R/W Circuit
DTC Circuit
ENTHRT
EN_ALL
Instruction Decoder
CLK
SZ
1/BW
BMF
Policing Logic
1506
PAF
Marker
CLK
SZ
BW
SP

FIG. 17

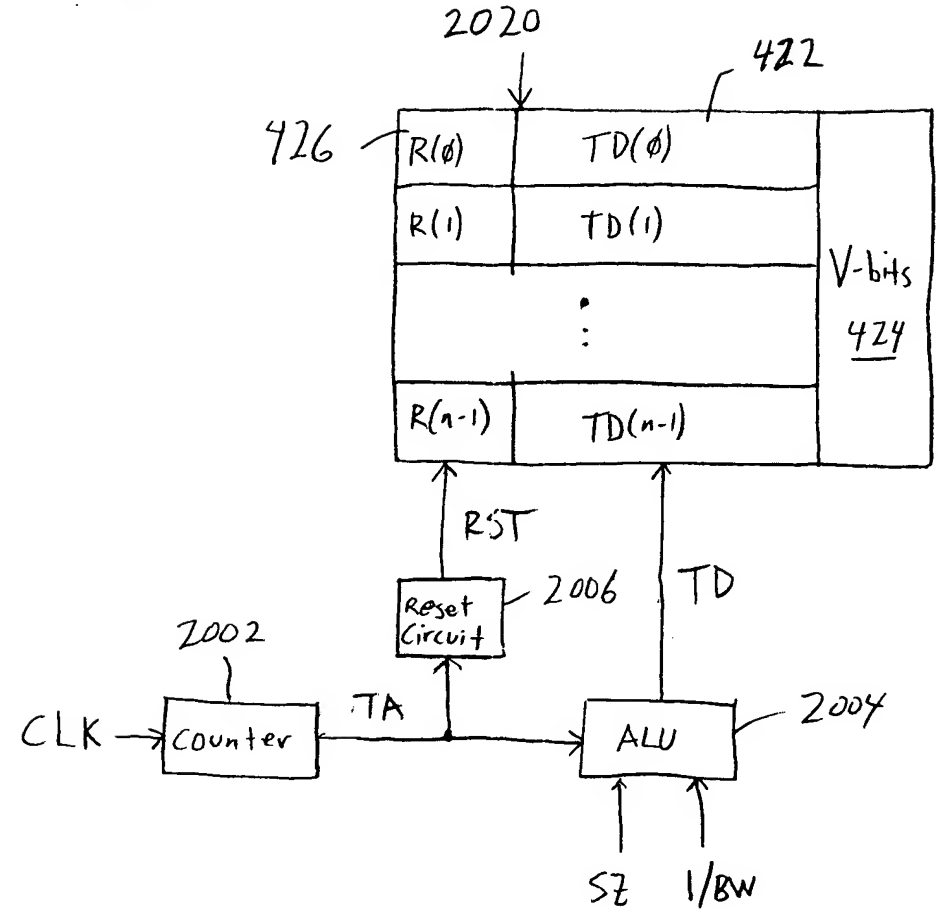
2000
2020
422
426
R(0)
TD(0)
R(1)
TD(1)
V-bits
424
R(n-1)
TD(n-1)
RST
TD
Reset Circuit
2006
2002
CLK
Counter
TA
ALU
2004
SZ
1/BW

FIG. 18